What is claimed is:

1. A delay locked loop (DLL) in a semiconductor device, comprising:

an clock buffer receiving an external clock signal and an inverted clock signal and outputting first and second internal clock signals to be used in the DLL circuit; and

a variable clock divider receiving the second internal signal from the clock buffer and variably dividing the second internal clock signal to have a predetermined pulse width according to a control signal based on a column address strobe (CAS) latency, which is set according to a frequency of the external clock signal, wherein the control signal is initially set to have a first logic level and is enabled to a second logic level when the CAS latency corresponds to a predetermined frequency.

2. The DLL as recited in claim 1, further comprising:

a plurality of delay lines, each delay line having a plurality of unit delay;

a phase comparator comparing a phase between a reference clock signal generated from the variable clock divider and a feedback signal;

a shift controller for generating a shift right signal or a shift left signal according to a comparison signal outputted from the phase comparator;

a shift register for adjusting amount of delay of the

delay lines in response to the shift right signal or the shift left signal; and

a delay model generating a feedback signal by compensating a time difference between the external clock signal and the internal clock difference.

3. The DLL as recited in claim 1, wherein the variable clock divider includes:

a first divider for generating a first divided signal having a first pulse width and a first period by receiving the second internal clock signal;

a second divider for generating a second divided signal having the first pulse width and a second period and a third divided signal having a second pulse width and the second period by receiving the first divided signal;

a selector for selectively outputting the second divided signal and the third divided signal in response to the control signal;

a third clock divider for generating a fourth divided clock signal having the first pulse width and a third period or a fifth divided clock signal having the second pulse width and the third period as a reference clock signal by receiving the second divided signal and the third divided signal; and

an output driver outputting an inverted reference clock signal into the delay lines.

4. The DLL as recited in claim 3, wherein the first

divider includes:

a 1^{st} NAND gate performing a NAND operation by receiving the second internal clock signal;

a 2^{nd} NAND gate performing a NAND operation by receiving the second internal clock signal;

a 1^{st} inverter inverting the second internal clock signal;

a 3^{rd} NAND gate performing a NAND operation by receiving an output signal of the 2^{nd} NAND gate;

a 4^{th} NAND gate, which is cross-coupled with the 3^{rd} NAND gate, outputting the first divided signal by performing a NAND operation for an output signal of the 1^{st} NAND gate;

a 5^{th} NAND gate performing a NAND operation by receiving output signals of the 3^{rd} NAND gate and the 1^{st} inverter;

a 6^{th} NAND gate performing a NAND operation by receiving output signals of the 4^{th} NAND gate and the 1^{st} inverter;

a 7^{th} NAND gate performing an NAND operation by receiving an output signal of the 6^{th} NAND gate and outputting an output signal to the 2^{nd} NAND gate; and

a 8^{th} NAND gate, which is cross-coupled with the 7^{th} NAND gate, performing a NAND operation by receiving an output signal of the 5^{th} NAND gate and outputting an output signal to the 1^{st} NAND gate.

5. The DLL as recited in claim 3, wherein the second divider includes:

a 9^{th} NAND gate for performing a NAND operation by

receiving the first divided signal;

a 10^{th} NAND gate for performing a NAND operation by receiving the first divided signal;

a 2^{nd} inverter inverting the first divided signal;

a 11^{th} NAND gate performing a NAND operation by receiving an output signal of the 10^{th} NAND gate;

a 12^{th} NAND gate, which is cross-coupled with the 11^{th} NAND gate, outputting the second divided signal by performing a NAND operation for an output signal of the 9^{th} NAND gate;

a 13^{th} NAND gate performing a NAND operation by receiving output signals of the 11^{th} NAND gate and the 2^{nd} inverter;

a 14^{th} NAND gate performing a NAND operation by receiving output signals of the 12^{th} NAND gate and the 2^{nd} inverter;

a 15^{th} NAND gate performing an NAND operation by receiving an output signal of the 14^{th} NAND gate and outputting an output signal to the 10^{th} NAND gate; and

a 16^{th} NAND gate, which is cross-coupled with the 15^{th} NAND gate, performing a NAND operation by receiving an output signal of the 13^{th} NAND gate and outputting an output signal to the 9^{th} NAND gate.

6. The DLL circuit as recited in claim 3, wherein the selector includes:

a first pass gate for passing the second divided signal to the second clock divider when the control signal is the first logic level, and for breaking the second divided signal when the control signal is the second logic level; and

a second pass gate for passing the third divided signal to the second clock divider when the control signal is the second logic level, and for breaking the second divided signal when the control signal is the first logic level.

7. The DLL circuit as recited in claim 3, wherein the third divider includes:

a 17^{th} NAND gate for performing a NAND operation by receiving an output signal of the selector;

a 18^{th} NAND gate for performing a NAND operation by receiving the output signal of the selector;

a 3^{rd} inverter inverting the output signal of the selector;

a 19^{th} NAND gate performing a NAND operation by receiving an output signal of the 18^{th} NAND gate;

a 20^{th} NAND gate, which is cross-coupled with the 19^{th} NAND gate, performing a NAND operation for an output signal of the 17^{th} NAND gate;

a 21^{st} NAND gate performing a NAND operation by receiving output signals of the 19^{th} NAND gate and the 3^{rd} inverter;

a 22^{nd} NAND gate performing a NAND operation by receiving output signals of the 20^{th} NAND gate and the 3^{rd} inverter and outputting a reference signal;

a 23^{rd} NAND gate performing an NAND operation by receiving an output signal of the 22^{nd} NAND gate and outputting an output signal to the 18^{th} NAND gate; and

a 24^{th} NAND gate, which is cross-coupled with the 23^{rd}

NAND gate, performing a NAND operation by receiving an output signal of the 21st NAND gate and outputting an output signal to the 17th NAND gate.